Attorney Docket No.: 2102397-992800

WHAT IS CLAIMED IS:

1. A memory device for interfacing with an integrated circuit communicating via a communication bus, said device comprising:

a decoding circuit for receiving communication signals received via the communication bus, for decoding the communication signals and for generating a plurality of protocol signals in response thereto;

a protocol select circuit for receiving said plurality of protocol signals; an array of memory cells;
a controller circuit for controlling the operation of said array of memory cells;

said protocol select circuit for configuring the controller circuit in response to the plurality of protocol signals.

- 2. The device of claim 1 wherein said memory cells are non-volatile memory cells.
- 3. The device of claim 2 wherein said protocol select circuit is a volatile storage element.
- 4. The device of claim 3 wherein said volatile storage element is a register.
- 5. The device of claim 3 wherein said volatile storage element is a flip-flop.
- 6. The device of claim 3 wherein said volatile storage element is an SRAM.
- 7. A memory device for interfacing with an integrated circuit communicating via an LPC bus, said circuit generating a start field, said device comprising:
- a decoding circuit for receiving the start field and for generating a plurality of protocol signals;

a protocol select circuit for receiving said plurality of protocol signals;

an array of non-volatile memory cells;

a controller circuit for controlling the operation of said array of non-volatile memory cells;

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said protocol select circuit for configuring the controller circuit in response to the plurality of protocol signals.

- 8. The device of claim 7 wherein said protocol select circuit is a flip-flop.
- 9. The device of claim 7 wherein said plurality of protocol signals represent protocol for LPC communication and for FWH communication.